library IEE;

use IEEE.STD\_LOGIC\_1664.all;

use IEEE.NUMERIC\_STD.all;

entity ALU4 is

port(a, b : in std\_logic\_vetcor(3 downto 0);

op : in std\_logic\_vetcor(2 downto 0);

r, m : out std\_logic\_vetcor(3 downto 0));

end ALU4;

architecture Behavioral of ALU4 is

signal s\_a, s\_b, s\_r : unsigned(2 downto 0);

signal s\_m : unsigned(7 downto 0);

benig

s\_a <= unsigned(a);

s\_b <= unsigned(b);

s\_m <= s\_a \* s\_b;

with op select

s\_r <= s\_a + s\_b when "000",

s\_a – s\_b when "001",

s\_m(3 downto 0) when "010",

s\_a / s\_b when "011",

s\_a rem s\_b when "100",

s\_a and s\_b when "101",

s\_a or s\_b when "110",

s\_a xor s\_b when "111";

r <= std\_logic\_vector(s\_r);

m <= std\_logic\_vector(s\_m(7 downto 4)) when (op = "010") else

(others => '0');

end Beahvioral;